



PATENT ABSTRACTS OF JAPAN

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// G01R 23/10(21) Application number: **11050135**(71) Applicant: **NEC CORP**(22) Date of filing: **26.02.99**(72) Inventor: **SAEKI TAKANORI**(54) **CLOCK PERIOD DETECTION CIRCUIT**

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(57) Abstract:

PROBLEM TO BE SOLVED: To provide a clock period detection circuit that can extend operating range of phase adjustment and multiplier circuit or the like by making rough period adjustment in advance.

SOLUTION: A plurality of delay detection circuits 2, whose delay times differ a little from each other, are connected in parallel to an input clock signal 1. A clock period is roughly detected for a short period by using signals identifying the delay detection circuits, through which a clock signal passes from those through which no clock signal passes, while the clock signal 1 is passed through the plural circuits 2. Thus, a configuration of rough adjustment of the period in advance is adopted, the operating range such as phase adjustment and multiplier circuits can be widened.

